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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,089	12/04/2001	Takahisa Hiraide	1075.1185	8026

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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/000,089	HIRAIDE ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-31 and 34-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3,5,6,9-29 and 31* is/are allowed.

6)☒ Claim(s) *2,4,30 and 34-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the applicant's amendment dated 8/17/2006.

The applicant has cancelled claims 7-8 and 32-33 in a previous amendment.

The applicant has added claims 34-36 as New Claims in the most recent amendment.

Claims 1, 3, 5-6, 9-29 and 31 were allowed in a previous office action.

Claims 1-6, 9-31, and 34-36 are pending in this office action.

Response to Amendment

1. Applicant's arguments filed 8/17/2006 have been fully considered but they are not persuasive.

As per claims 2 and 30, and as for claim 4 being dependent on claim 2:

The Applicant has submitted that the mask 105 of Rearick "does not convert the indeterminate values of the scan registers into a value at all, but merely precludes the indeterminate values from being sent to the signature analyzer 104" (Remarks, page 10). The applicant, in claim 2, specifies that the mask converts an indeterminate value from the scan registers to the MISR, "into a state value of "0" or "1", to mask" the undetermined values. The examiner submits that Rearick, in column 6 lines 11-17, states *the same limitation almost verbatim*. The examiner, in view of the applicant's limitation, has chosen to examiner only the "0" choice given by the applicant. And, as it is well known that a "mask" will change the output of a masked bit to a "0" using a "0" mask bit, the "undetermined value" from the scan registers will be changed to "0" by

Rearick, which meets the requirements of claim 2. The examiner would like to refer the applicant to the definition of "mask" at http://www.answers.com/mask&r=67, where it is defined as: "A pattern of bits used to accept or reject bit patterns in another set of data. For example, the Boolean AND operation can be used to match a mask of 0s and 1s with a string of data bits. When a 1 occurs in both the mask and the data, the resulting bit will contain a 1 in that position". Conversely, when a mask of 0 occurs in the mask, the resulting bit will always be 0 in that position. Since the examiner has chosen to examiner the "0" alternative of the applicant's claim, the examiner rejects that applicant's argument as unpersuasive because Rearick teaches a "0" output because the definition of "mask" is well known to produce such an output.

Also argued in the Remarks is that the signature analyzer 104 of Rearick "performs no verification of output results in which said indeterminate value is masked, but merely generates a signature. Further, even if it were assumed, arguendo, that this signature generation could be a verification process, the signature is generated without signals that were indeterminate, because the mask causes them to be ignored (Column 6, Lines 11-14), rather than generating the signature with converted values in place of the indeterminate values". The examiner respectfully disagrees because, as in the above, the examiner has shown that the *determinate* result of the mask register is an input to the MISR of "0". And, the examiner also disagrees with the applicant's "verification of output results argument" because the applicant, in the Disclosure page 4, lines 15-27, has described the verifier of the applicant's invention to be a MISR, therein defining a "verifier" as a MISR. And, as the examiner has pointed out above in regard to

a determinate mask output value, and also in view of the applicant's own definition of a verifier, the examiner responds that this part of the applicant's argument is unpersuasive.

Therefore the examiner maintains the rejections of claims 2, 4 and 30 under 35 USC 102(e) as being anticipated by Rearick, and as outlined in the previous office action.

Claim Rejections - 35 USC § 102 (New)

2. Claims 34-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Rearick, U.S. Patent No. 6715105.

As per claim 34:

Rearick teaches a testing apparatus for an integrated circuit comprising: a plurality of shift registers, to which test patterns are inputted (FIG. 3 172), configured with sequential circuit elements inside said integrated circuit (FIG. 1,2,3 scan chains); a mask (FIG. 2,3 105) to specify a shift register in said plurality of shift registers (out of a choice of scan_out 0...n as in FIG. 3) which outputs an indeterminate value (see column 6 lines 11-17), based on external control signals (column 8 liners 60-67), and to convert the indeterminate value, contained in the outputs from the specified shift register (scan chain 0...n), into a state value of "0" [~~or "1"~~] to mask the indeterminate value (see column 6 lines 11-17); and an output verifier (FIG. 3 104) to verify the masked output results of the specified shift register, from which output results the indeterminate value is excluded (see column 6 lines 11-17).

As per claim 35:

Rearick further teaches the testing apparatus according to claim 34, wherein said output verifier includes a compressing means for compressing the masked outputs (column 8 lines 4-11).

As per claim 36:

Rearick teaches an integrated circuit including sequential circuit elements (FIG. 1,2,3 scan chains), comprising: a plurality of shift registers (FIG. 1,2,3 scan chains), to which test patterns are inputted (FIG. 2 SDI 122), configured with said sequential circuit elements; a mask (FIG. 2,3 105) to specify a shift register in said plurality of shift registers (out of a choice of scan_out 0...n as in FIG. 3) which outputs an indeterminate value (see column 6 lines 11-17), based on external control signals (column 8 liners 60-67), and to convert the indeterminate value, contained in the outputs from the specified shift register (scan chain 0...n), into a state value of "0" [~~or "1"~~] to mask the indeterminate value (see column 6 lines 11-17); and an output verifier (FIG. 3 104) to verify the masked output results of the specified shift register, from which output results the indeterminate value is excluded (see column 6 lines 11-17).

Conclusion

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John P Trimmings
Examiner
Art Unit 2138

jpt

GUY LAMARRE
PRIMARY EXAMINER